FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-23005-3E

ASSP
CMOS

3 V Single Power Supply Audio Interface Unit (AIU)

MB86437

■ DESCRIPTION

The FUJITSU MB86437 is an AIU (audio interface unit) LSI for +3 V single-power source digital telephone devices, manufactured using CMOS process technology. The codec transmission filter characteristics meet G.712 standards, and can handle input and output in A-Law, μ-Law and linear conversion modes. The MB86437 also contains the necessary DTMF, microphone and receiver amps for telephone devices.

■ FEATURES

- +3 V single power supply
- Low power consumption: muting settings for each operating mode
  Normal operation : 5.0 mA TYP
  Standby mode : 0.5 μA TYP
- On-chip codec filter meets G.712 standards
- Selection of codec companding law (A-law, μ-law, 14 bit linear)
- On-chip low-noise microphone amp (2-channel) (0 to 35 dB amplification)
- On-chip receiver speaker amps (32 Ω BTL type: 10 mW MIN)
- On-chip earphone speaker amps (32 Ω single type: 5 mW MIN)

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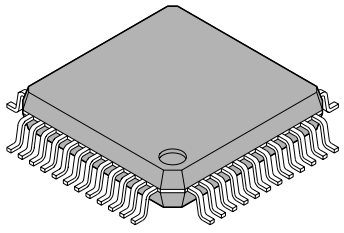
■ PACKAGE

48 pin, Plastic LQFP



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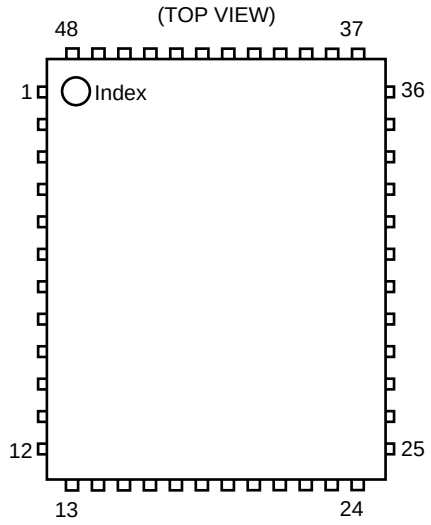
- On-chip electronic volume gain adjustments (sending, receiving, tone)
- On-chip accessory input/output circuits
- DTMF generator function
- Service tone generation
- CMOS compatible input/output

■ PIN ASSIGNMENT



(FPT-48P-M05)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	A/D	Description
1	SWI	I/O	A/D	I/O pin for analog switch SW12 The standard on resistance for the analog switch is 500 Ω.
2	SWO	I/O	A/D	I/O pin for analog switch SW12 Connected to pin 1 via switch SW12.
3	RAUD	O	A	Output pin for the received audio signal to the external speaker or for testing.
4	VD1	P	A	Power supply pin for reception. Supply a voltage between 2.7 V and 3.6 V.
5	JEAR	O	A	Amplifier output pin for the earphone speaker. Can output 5 mW for a 32 Ω load.
6	EAR	O	A	Amplifier output pin for the receiver speaker. Internal BTL connection to XEAR. The maximum output for a 32 Ω load between EAR and XEAR is 10 mW.
7	XEAR	O	A	Amplifier output pin for the receiver speaker. BTL connection to XEAR.
8	VS1	G	A	Ground pin for reception. Set to 0 V.
9	TONE	O	A	Amplifier output pin for the tone speaker. The output can be set to normal mode, ground, or high impedance.
10	TBO	O	A	AMP4 output pin. Pair high pass filter with TBI so that there is no DC offset at the speaker.
11	TBI	I	A	AMP4 inverted (–) input pin
12	PTBO	O	A	PCM reception, tone addition output
13	MDI	I	A	Pin used to add an analog input signal to the tone section or apply an envelope to the tone. Required functions can be selected by controlling SW16. Setting SW16 off sets the input impedance to approximately 140 kΩ and setting SW16 on sets the input impedance to approximately 210 kΩ.
14	VD2	P	A	Power supply pin for reception. Supply a voltage between 2.7 V and 3.6 V.
15	DSCK	I/O	A	Can be connected to EXSD and TAUD by path switching.
16	EXSD	I/O	A	Can be connected to DSCK and TAUD by path switching.
17	TAUD	I/O	A	Can be connected to EXSD and DSCK by path switching.
18	MICO	O	A	Output pin for mike amplifier [1]
19	MIC	I	A	Inverted input pin (–) for mike amplifier [1]
20	XMIC	I	A	Non-inverted input pin (+) for mike amplifier [1]
21	JMIC	I	A	Inverted input pin (–) for mike amplifier [2]
22	JMICO	O	A	Output pin for mike amplifier [2]
23	VS2	G	A	Ground pin for transmission. Set to 0 V.
24	SGC	O	A	Pin for connecting the bypass capacitor for the signal ground potential generation circuit. Connect a capacitor between SGC and VS2.
25	VS4	G	A	Ground pin for A/D and D/A. Set to 0 V.
26	SGI	I	A	General-purpose amplifier. To use, connect to SGO.

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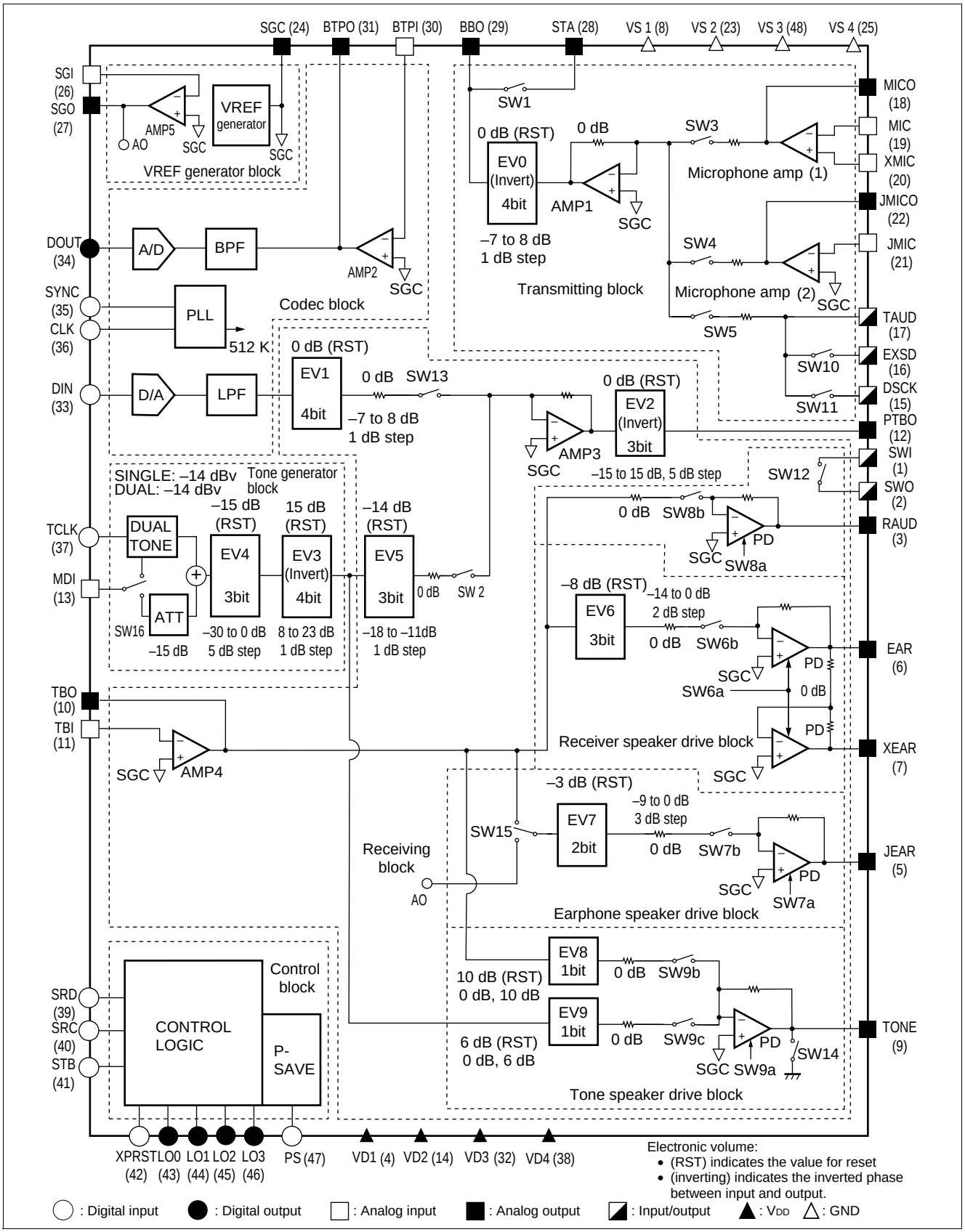
Pin No.	Symbol	I/O	A/D	Description
27	SGO	O	A	General-purpose amplifier output pin. The signal can also go to JEAR via SW15.
28	STA	O	A	Transmission analog signal output via SW1. Connect to AMP4 when performing sidetone addition for reception. The standard on resistance for the analog switch is 500 Ω.
29	BBO	O	A	Transmission analog signal output pin
30	BTPI	I	A	Inverted input pin (–) for the PCM ENCODE section input op-amp
31	BTPO	O	A	Output pin for the PCM ENCODE section input op-amp
32	VD3	P	D	Power supply pin for transmission. Supply a voltage between 2.7 V and 3.6 V.
33	DIN	I	D	PCM signal input pin. The signal is clocked in on the falling edge of CLK. CMOS interface.
34	DOUT	O	D	PCM signal output pin. The signal is clocked out on the rising edge of CLK. After data output, becomes fixed at the "H" level if PLL synchronization is lost or a power-down occurs. CMOS interface.
35	SYNC	I	D	Transmission and reception sync signal input pin for the PCM CODEC section. The operating clock frequency is 8 kHz. CMOS interface. Fixing at "H" or "L" causes part of the CODEC section to power-down.
36	CLK	I	D	Input pin for setting the bit rate for the transmission and reception PCM signals. The data rate can be selected from 64 kHz to 3.152 MHz for μ-law or A-law operation, or from 128 kHz to 3.152 MHz for linear operation. Fixing at "H" or "L" causes part of the CODEC section to power-down. CMOS interface.
37	TCLK	I	D	Clock input pin for tone generation. The internal clock divided by one or two (set by D_4D_3 of address 01110) can be used as the tone CLK. CMOS interface.
38	VD4	P	D	Digital power supply pin. Supply a voltage between 2.7 V and 3.6 V.
39	SRD	I	D	10-bit serial data input pin. CMOS interface. This data sets the electronic volume, path, and tone settings.
40	SRC	I	D	Write clock input pin for the 10-bit serial data. CMOS interface. SRD is clocked in the rising edge.
41	STB	I	D	Strobe signal for the serial data latch. Latches on "L". CMOS interface.
42	XPRST	I	D	Reset signal input pin for the digital circuits. CMOS interface. L: Initialize internal latches. H: Normal
43	LO0	O	D	Latch output pin for external control. Outputs D_0 of address 01000. CMOS interface.
44	LO1	O	D	Latch output pin for external control. Outputs D_1 of address 01000. CMOS interface.
45	LO2	O	D	Latch output pin for external control. Outputs D_2 of address 01000. CMOS interface.
46	LO3	O	D	Latch output pin for external control. Outputs D_3 of address 01000. CMOS interface.
47	PS	I	D	Power-down control signal input pin. CMOS interface. Powers down all circuits regardless of register settings.
48	VS3	G	D	Digital ground pin. Set to 0 V.

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. Register Settings

The MB86437 IC chip controls all electronic volume, switch, tone generator circuit and power-down control circuit by means of the SRD, STB and SRC input.

(1) Mode setting

The data format consists of 10 bits of serial data. The first 5 bits (A_4 to A_0) are the address and the next 5 bits (D_4 to D_0) are data. SRD is clocked in on the rising edge of SRC and latched when STB is "L". During power-down, the register is not reset and writing to the register is possible. A reset and data initialization occurs when XPRST is "L".

Data	Address	Meaning	Data Setting After a Reset					Data Meaning				
			D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0
A00	00000	Test mode	0	0	0	0	0	00000: Normal operation (writing prohibited)				
A01	00001	EV0 gain	0	1	1	1	X	EV0 [0000: –7 dB to 1111: 8 dB, step 1 dB, Reset: 0 dB]				X
A02	00010	EV1 gain	0	1	1	1	X	EV1 [0000: –7 dB to 1111: 8 dB, step 1 dB, Reset: 0 dB]				X
A03	00011	EV2 gain	X	X	0	1	1	X	X	EV2 [000: –15 dB to 111: 15 dB, step 5 dB, Reset: 0 dB]		
A04	00100	Transmit mute 1 (SW3, 4, 5) Receive mute 1 (SW6b, 7b, 8b, 9b, 9c)	0	X	X	X	0	Receive mute (SW6b, 7b, 8b, 9b, 9c) 1: Mute 1 0: No mute	X	X	X	Transmit mute (SW3, 4, 5) 1: Mute 1 0: No mute
A05	00101	SW8, 3, 4, 5 mute 2	1	X	1	1	1	SW8 1: Mute 2 0: No mute Valid when D_4 of A04 is "0"	X	SW3 1: Mute 2 0: No mute	SW4 1: Mute 2 0: No mute	SW5 1: Mute 2 0: No mute
										Valid when D_0 of A04 is "0"		
A06	00110	EV7 gain/SW7b, 9b, 9c, 6b mute 2	1	0	1	1	1	EV7 [00: –9 dB to 11: 0 dB, step 3 dB, Reset: –3 dB]		SW7b 1: Mute 2 0: No mute	SW9b9c 1: Mute 2 0: No mute	SW6b 1: Mute 2 0: No mute
										Valid when D_4 of A04 is "0"		
A07	00111	SW2, 11, 12, 10 control	X	1	0	0	0	X	SW2 1: ON 0: OFF	SW11 1: ON 0: OFF	SW12 1: ON 0: OFF	SW10 1: ON 0: OFF
A08	01000	Digital parallel output	X	0	0	0	0	X	L03	L02	L01	L00
A09	01001	EV3 gain	0	1	1	1	X	EV3 [0000: 8 dB to 1111: 23 dB, step 1 dB, Reset: 15 dB]				X

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Data	Address	Meaning	Data Setting After a Reset					Data Meaning				
			D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0
A0A	01010	Tone [1] setting	0	0	0	0	0	Tone 1 waveform 1: Square wave 0: Sine wave	$na = a_7 \times 2^7 + a_6 \times 2^6 + \ldots + a_1 \times 2 + a_0$			
									a_7	a_6	a_5	a_4
A0B	01011		X	0	0	1	0	X	a_3	a_2	a_1	a_0
A0C	01100	Tone [2] setting	0	0	0	0	0	Tone 2 waveform 1: Square wave 0: Sine wave	$nb = b_7 \times 2^7 + b_6 \times 2^6 + \ldots + b_1 \times 2 + b_0$			
									b_7	b_6	b_5	b_4
A0D	01101		X	0	0	1	0	X	b_3	b_2	b_1	b_0
A0E	01110	Tone waveform setting (for tones [1] and [2])	0	0	X	0	0	Divide ratio (TCLK/N): 00 TCLK/1; 01 TCLK/1; 10 TCLK/2; 11 Use prohibited	Division ratio (M): 12 divisions; 24 divisions; 24 divisions; Use prohibited	X	Tone [1] control 1: Generate 0: Stop	Tone [2] control 1: Generate 0: Stop
A0F	01111	CODEC compression rule	X	X	X	0	0	X	X	X	CODEC companding law 00: μ-LAW 01: Linear 10: A-LAW 11: Use prohibited	
A10	10000	PD control and SW14 control for CODEC, TONE, SGO, and transmission (TX)	0	0	0	0	0	CODEC PD 1: PD 0: Operate	TONE PD 1: PD 0: Operate	SGO PD 1: PD 0: Operate	Transmitter PD 1: PD 0: Operate	SW14 1: TONE output 0 V 0: Operate
A11	10001	PD control for RAUD, JEAR, TONE, and EAR	0	X	0	0	0	RAUD PD (SW8a) 1: Independent 0: Linked	X	JEAR PD (SW7a) 1: Independent 0: Linked	TONE PD (SW9a) 1: Independent 0: Linked	EAR PD (SW6a) 1: Independent 0: Linked
								Independent: Do not power-down corresponding amplifier in conjunction with mute. Linked: Power-down corresponding amplifier in conjunction with mute.				
A12	10010	DOUT/SW1, 13, 9b, 9c	0	0	0	1	1	DOUT 1: Fixed at "H" 0: Operate	SW1 mute 1: Mute 0: No mute	SW13 mute 1: Mute 0: No mute	SW9b mute 0: Mute 1: No mute	SW9c mute 0: Mute 1: No mute

The tone frequencies are as follows. (f_a and f_b are the frequencies of tones [1] and [2] respectively.)
(f_{in} = TCLK input frequency (512 kHz recommended when N = 1, M = 12, 1024 kHz recommended when N = 1, M = 24 $\rightarrow$ $f_{in}/(N \times M)$ = 42.667 kHz), N: Divide ratio (1 or 2), M: Number of divisions (12 or 24))
$f_a = (f_{in}/(N \times M))/(n_a + 1)$, $f_b = (f_{in}/(N \times M))/(n_b + 1)$

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Data	Address	Meaning	Data Setting After a Reset					Data Meaning				
			D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0
A13	10011	EV8, EV6 gain	1	X	0	1	1	EV8 gain 1: 10 dB 0: 0 dB	X	EV6 [000: –14 dB to 111: 0 dB, step 2 dB, Reset: –8 dB]		
A14	10100	EV4 gain	X	X	0	1	1	X	X	EV4 [000: –30 dB to 111: 0 dB, step 5 dB, Reset: –15 dB]		
A15	10101	EV9, EV5 gain	1	X	0	1	1	EV9 gain 1: 6 dB 0: 0 dB	X	EV5 [000: –11 dB to 111: –18 dB, step 1 dB, Reset: –14 dB]		
A16	10110	SW15, 16 control	X	X	X	0	0	X	X	X	SW15 1: AMP5 0: AMP4	SW16 * 1 1: Envelope 0: ATT
A17	10111	All PD	X	X	X	X	1	X	X	X	X	All circuits PD 1: Normal 0: PD

Notes: 1. When unused, connect the MDI input to OPEN or SGC. When using ATT, an SGC-centered signal or capacitive coupling is required (to prevent an offset).
2. Set X to 0.
3. Set to initial value by a reset (____ section).

(2) Transmitting audio mute settings

Switches SW1, SW3, SW4, SW5, SW10, and SW11 have the following functions. Address 00100 signals have priority.

Setting					Switching setting						Remarks
Address	A_4 to A_0	A_4 to A_0	A_4 to A_0	A_4 to A_0							
	00100	00101	00111	10010							
Data bit	D_4 to D_0	D_4 to D_0	D_4 to D_0	D_4 to D_0	SW1	SW3	SW4	SW5	SW10	SW11	
	– * * * 1	– * – – –	* – – – –	– – – – –	—	×	×	×	—	—	Microphone amp [1], [2] mute Microphone amp [2] mute Microphone amp [1] mute
	– * * * 0	– * 0 1 –	* – – – –	– – – – –	—	○	×	—	—	—	
	– * * * 0	– * 1 0 –	* – – – –	– – – – –	—	×	○	—	—	—	
	– * * * 0	– * – – 0	* – 0 – 0	– – – – –	—	—	—	○	×	×	
	– * * * 0	– * – – 1	* – 0 – 1	– – – – –	—	—	—	×	○	×	
	– * * * 0	– * – – 1	* – 1 – 0	– – – – –	—	—	—	×	×	○	
	– * * * –	– * – – –	* – – – –	– 1 – – –	×	—	—	—	—	—	

○ : ON, × : OFF, — : not determined

(3) Receiving audio mute settings

Switches SW6b, SW7b, SW8b, SW9b, SW9c, and SW12 have the following functions. Address 00100 signals have priority.

Setting						Switching setting						Remarks
Address	A_4 to A_0	A_4 to A_0	A_4 to A_0	A_4 to A_0	A_4 to A_0							
	00100	00101	00110	00111	10010							
Data bit	D_4 to D_0	D_4 to D_0	D_4 to D_0	D_4 to D_0	D_4 to D_0	SW6b	SW7b	SW8b	SW9b	SW9c	SW12	
	1 * * * –	– * – – –	– – – – –	* – – – –	– – – – –	×	×	×	×	×	—	
	0 * * * –	1 * – – –	– – – – –	* – – – –	– – – – –	—	—	×	—	—	—	
	0 * * * –	0 * – – –	– – 1 – –	* – – – –	– – – – –	—	×	○	—	—	—	
	0 * * * –	– * – – –	– – 0 1 –	* – – – –	– – – – –	—	○	—	×	×	—	
	0 * * * –	– * – – –	– – – 0 –	* – – – –	– – – 0 1	—	—	—	×	○	—	
	0 * * * –	– * – – –	– – – 0 –	* – – – –	– – – 1 0	—	—	—	○	×	—	
	0 * * * –	– * – – –	– – – – 1	* – – – –	– – – – –	×	—	—	—	—	—	
	0 * * * –	– * – – –	– – – – 0	* 0 – – –	– – – – –	○	—	—	—	—	×	
	0 * * * –	– * – – –	– – – – –	* 1 – – –	– – – – –	—	—	—	—	—	○	

○ : ON, × : OFF, — : not determined

(4) Electronic volume controls

There are ten different electronic volume controls, EV0 through EV9, with the following specifications. Electronic volume control settings are made by the SRD, SRC and STB signals, and setting values are reset by the XPRST signal.

Table 1 Relation of Volume Control Data bit Values to Gain

Code	Address / Data	00001	00010	00011	01001	10100	10101	10011	00110	10011	10101	Unit
		EV0	EV1	EV2	EV3	EV4	EV5	EV6	EV7	EV8	EV9	
	$D_4 D_3 D_2 D_1 D_0$	Inverted	Non-Inverted	Inverted	Inverted	Non-Inverted	Non-Inverted	Non-Inverted	Non-Inverted	Non-Inverted	Non-Inverted	
		D_4 to D_1	D_4 to D_1	D_2 to D_0	D_4 to D_1	D_2 to D_0	D_2 to D_1	D_2 to D_0	D_4 to D_3	D_4	D_4	
0	0 0 0 0 0	–7	–7	–15	8	–30	–11	–14	–9	0	0	
1	0 0 0 0 1			–10		–25	–12	–12	–9	0	0	
2	0 0 0 1 0	–6	–6	–5	9	–20	–13	–10	–9	0	0	
3	0 0 0 1 1			0		–15	–14	–8	–9	0	0	
4	0 0 1 0 0	–5	–5	5	10	–10	–15	–6	–9	0	0	
5	0 0 1 0 1			10		–5	–16	–4	–9	0	0	
6	0 0 1 1 0	–4	–4	15	11	0	–17	–2	–9	0	0	
7	0 0 1 1 1			15		0	–18	0	–9	0	0	
8	0 1 0 0 0	–3	–3		12				–6			
9	0 1 0 0 1								–6			
10	0 1 0 1 0	–2	–2		13				–6			
11	0 1 0 1 1								–6			
12	0 1 1 0 0	–1	–1		14				–6			
13	0 1 1 0 1								–6			
14	0 1 1 1 0	0	0		15				–6			
15	0 1 1 1 1								–6			
16	1 0 0 0 0	1	1		16		–11	–14	–3	10	6	dB
17	1 0 0 0 1						–12	–12	–3	10	6	
18	1 0 0 1 0	2	2		17		–13	–10	–3	10	6	
19	1 0 0 1 1						–14	–8	–3	10	6	
20	1 0 1 0 0	3	3		18		–15	–6	–3	10	6	
21	1 0 1 0 1						–16	–4	–3	10	6	
22	1 0 1 1 0	4	4		19		–17	–2	–3	10	6	
23	1 0 1 1 1						–18	0	–3	10	6	
24	1 1 0 0 0	5	5		20				0			
25	1 1 0 0 1								0			
26	1 1 0 1 0	6	6		21				0			
27	1 1 0 1 1								0			
28	1 1 1 0 0	7	7		22				0			
29	1 1 1 0 1								0			
30	1 1 1 1 0	8	8		23				0			
31	1 1 1 1 1								0			

Notes: • Each setting value is determined in relation to the initial setting value.
• Returns to initial value at reset (——— parts)
• The "Inverted" and "Non-Inverted" columns indicate the I/O phase.
• Settings with no gain figure listed are undefined.

(5) Tone generation circuit

This section describes the frequency settings and output control.

- **Tone frequency control register**

The clock used to generate tones is the clock input from TCLK divided by 1 or 2. The divide ratio is set by the data at address 01110. Also, 12 division and 24 division modes are available to generate a smooth frequency even at low frequencies.

Table 2 Register Control for the TONE Clock Frequency

Address 01110		Tone Generation Clock (f_{IN})	Waveform Division
D_4	D_3		
0	0	Frequency input to TCLK	12 divisions
0	1	Frequency input to TCLK	24 divisions
1	0	Frequency input to TCLK divided by 2	24 divisions
1	1	Prohibited	

The following formula specifies the frequencies that can be set by the tone frequency control register.
Set frequency $f = f_{IN}/(M \times (1 + n))$, M = division mode (12 or 24)
n = 4, 5, ..., 255 (f_{IN}: Tone generation clock)
f_{IN} = 4 MHz max.

Therefore, the range of available frequencies in 12 division mode and f_{IN} = 512 kHz, and in 24 division mode and f_{IN} = 1024 kHz is:
f_{min} = 167 Hz, f_{max} = 8533 Hz

Table 3 lists the frequency settings for all the standard DTMF frequencies.

Table 3 Tone Frequency Register Control

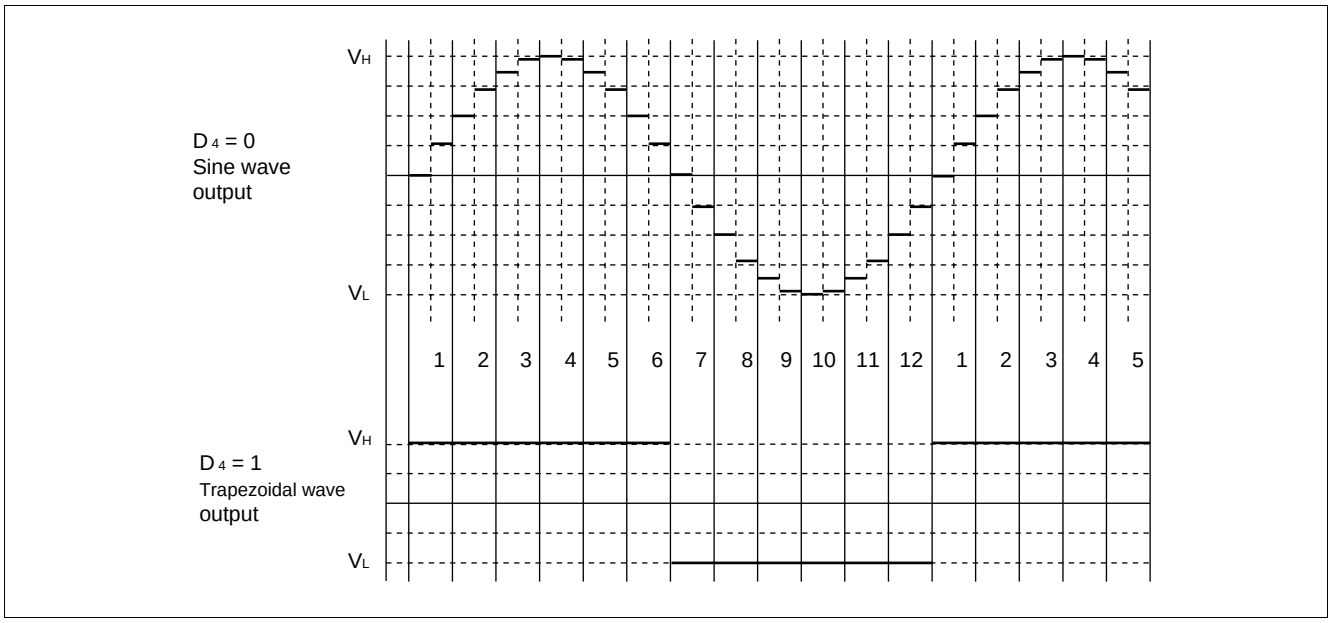
(Setting: 12 divisions and f_{IN} = 512 kHz, or 24 divisions and f_{IN} = 1024 kHz)

Tone Type		Standard Frequency (Example of generated frequency)	Set Frequency	Address 01010/01100 Data					Address 01011/01101 Data					n	Error
				D_4	D_3	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_0		
Service tones (Single tone)		400 Hz	398.7 Hz	—	0	1	1	0	*	1	0	1	0	106	–0.32%
		2000 Hz	2031.7 Hz	—	0	0	0	1	*	0	1	0	0	20	1.56%
DTMF	Low tones	697 Hz	699.4 Hz	—	0	0	1	1	*	1	1	0	0	60	0.34%
		770 Hz	775.7 Hz	—	0	0	1	1	*	0	1	1	0	54	0.74%
		852 Hz	853.3 Hz	—	0	0	1	1	*	0	0	0	1	49	0.15%
		941 Hz	948.1 Hz	—	0	0	1	0	*	1	1	0	0	44	0.75%
	High tones	1209 Hz	1219.0 Hz	—	0	0	1	0	*	0	0	1	0	34	0.82%
		1336 Hz	1333.3 Hz	—	0	0	0	1	*	1	1	1	1	31	–0.20%
		1477 Hz	1471.3 Hz	—	0	0	0	1	*	1	1	0	0	28	–0.38%
		1633 Hz	1641.0 Hz	—	0	0	0	1	*	1	0	0	1	25	0.48%

Notes: • Settings are shown in binary notation.
• Error is the error between the set frequency and standard frequency.
• Set n to 4 or higher and set a frequency of 5 kHz or less.

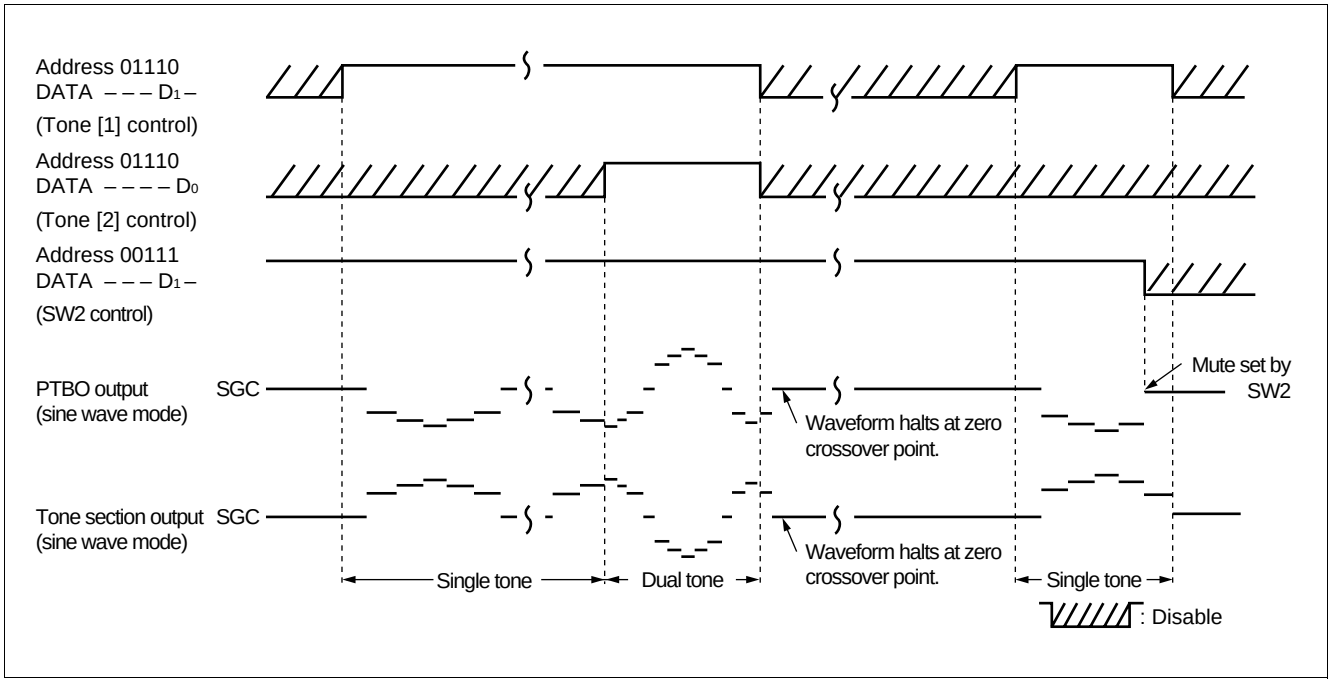
- **Tone output waveform**

The D_4 data bit at address 01010, 01100 may be used to select either sine-wave or trapezoidal waveforms for tone output.



- **Tone output control**

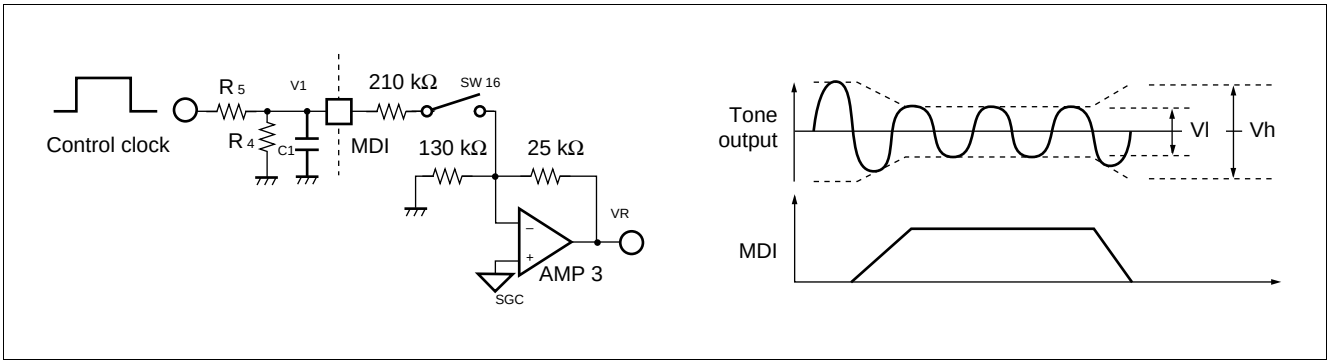
Tone output is controlled by addresses 01110 and 00111. Provided TCLK does not stop, sine wave output always halts close to zero. Also, SW2 controls output muting.



- **Tone envelope**

Even if the tone halts at close to zero, changes in the DC voltage can still occur can be audible. Using SW16 for tone control enables the voltage level for tone generation to be controlled. The waveform amplitude characteristics have the following general relationships.

Va = 2 × (0.47 – 0.12 × Vl) (Vl: MDI voltage, Va = Tone amplitude)



For a cut off frequency of 8.3 Hz, control clock of 0 to 3 V, and SGC = 1.5 V, the envelope ratio and resistor and capacitor values are as follows.

Envelope Ratio Aim Value	Recommended Values			Vh, Vl Voltages		Envelope Ratio Calculated Value
	R4	R5	C1	Max. (Vh)	Min. (Vl)	
–3 dB	33 kΩ	22 kΩ	1.5 µF	0.828 V	0.584 V	–3.13 dB
–4 dB	47 kΩ	18 kΩ	1.5 µF	0.824 V	0.516 V	–4.05 dB
–5 dB	82 kΩ	15 kΩ	1.5 µF	0.810 V	0.448 V	–5.15 dB
–6 dB	270 kΩ	15 kΩ	1.5 µF	0.790 V	0.400 V	–5.91 dB

(6) CODEC I/O

Code companding for μ-law and A-law is in accordance with CCITT Recommendation G.711.
Linear coding uses 14-bit, two's complement code which is output MSB-first.
Address 01111 is used to control μ-law, A-law, and linear code I/O.

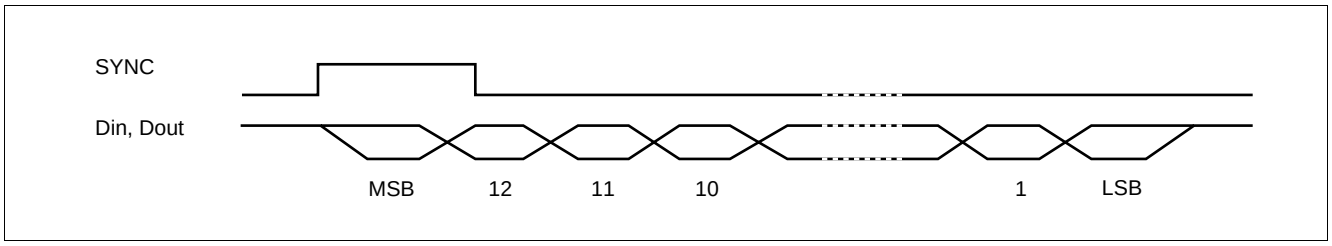
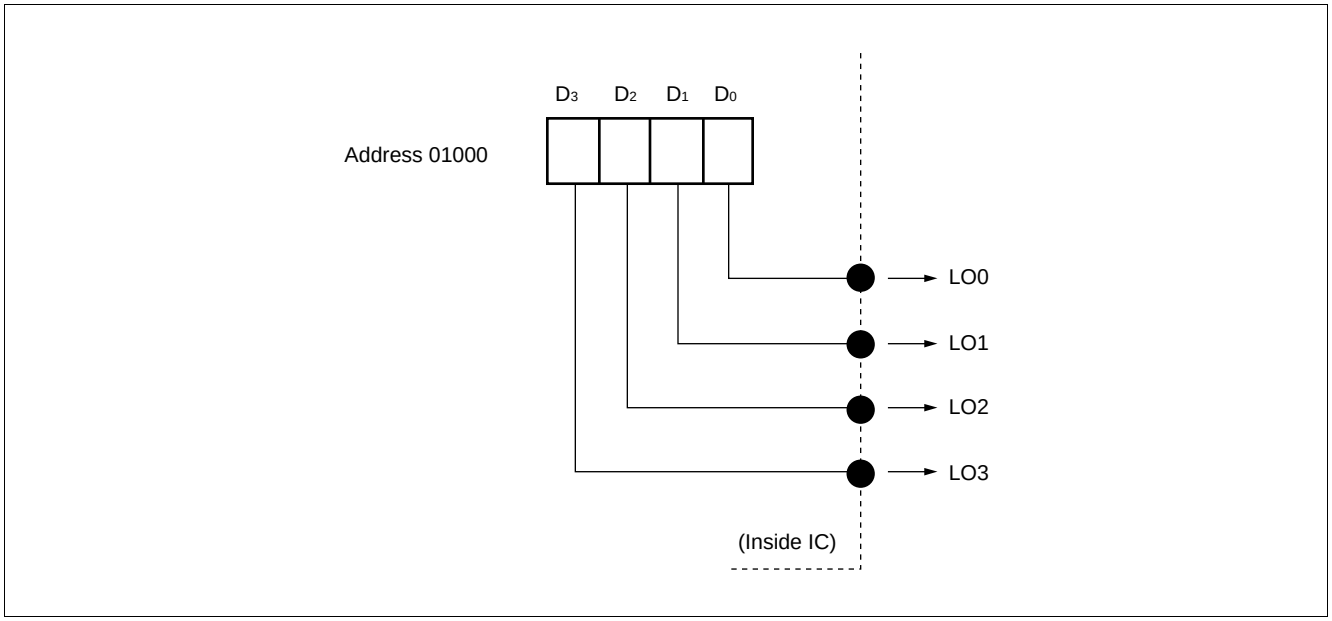


Table 4 Table of Linear Code vs. Voltage

MSB Code LSB	PTBO Standard Voltage (V)
0 1 1 1 1 1 1 1 1 1 1 1 1 1	2.2647
to	to
0 0 0 0 0 0 0 0 0 0 0 0 0 1	1.5009
0 0 0 0 0 0 0 0 0 0 0 0 0 0	1.5000
1 1 1 1 1 1 1 1 1 1 1 1 1 1	1.4991
to	to
1 0 0 0 0 0 0 0 0 0 0 0 0 1	0.7354

(7) Parallel output

LO0 to 3 are general-purpose latch outputs for external control. LO0 to 3 output the data written to address 01000. The outputs are CMOS outputs. Data output continues during power-down.

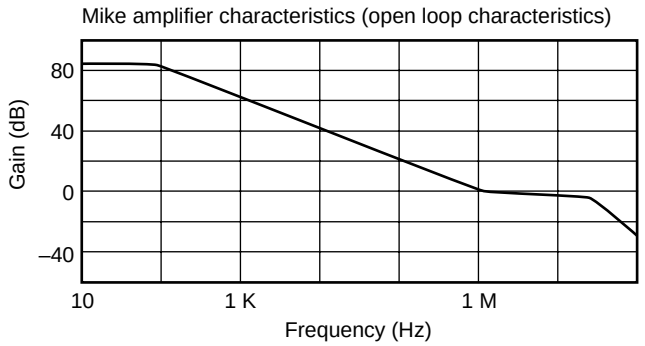


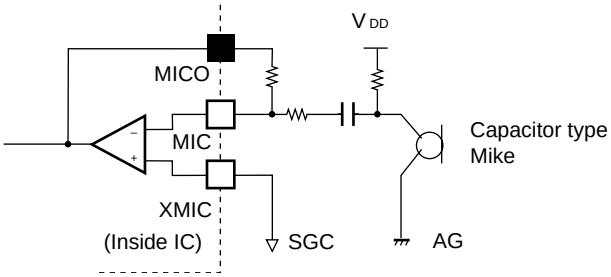
2. Analog Input

Analog inputs in the MB86437 include the two microphone inputs and the three accessory input.

(1) Microphone amps

The microphone amps take the incoming signal from the microphones and amplify it to any desired level of gain. The microphone amps are low-noise types for use with capacitor microphones, and are capable of a wide range of amplification. All microphone amps must be AC coupling with capacitors to prevent amplification of DC offset level.





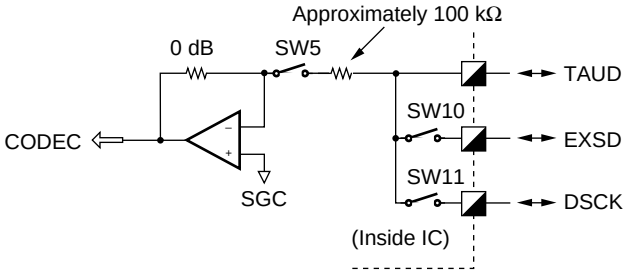
(2) Accessory input

Direct input from the TAUD to the codec unit is possible through SW5, without passing through the microphone amp. Care must be taken with the input signal in this case, however, because input resistance is not at high-impedance level.

Microphone amp output may be added to the signal by using switching controls.

In this case, the result will be at the additional output level.

In addition, SW10 and SW11 may be used to transmit digital data from the TAUD to EXSD and DSCK, allowing the sending of fax or PC data without modification.



Note: TAUD, EXSD, and DSCK contain no buffers. If not used, TAUD, EXSD and DSCK should be connected to SGC.

3. Analog Output Relationships

The four analog outputs consist of three speaker drivers (for receiver, earphone, and tone) and an accessory output.

(1) Speaker driver amps

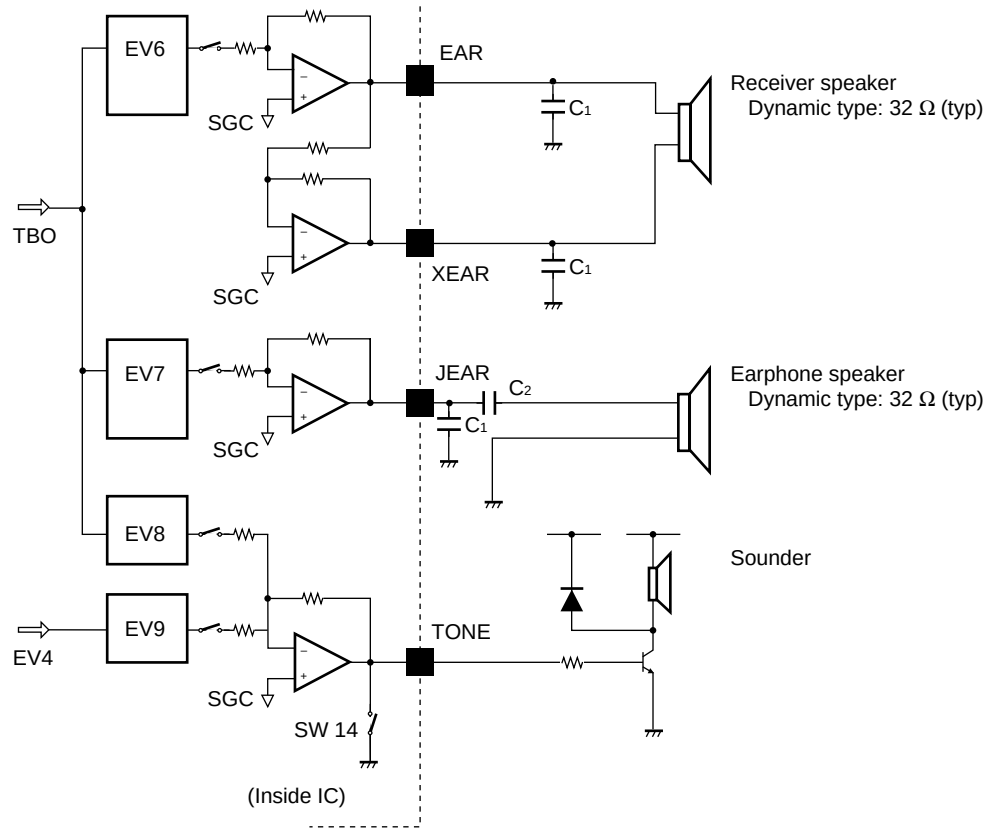
The speaker driver amps consist of one BTL output (the receiver output) and one single output (the earphone output). Also, the sounder driver consists of one single output and the sounder output can be obtained via a transistor. As the speaker amps have high power consumption, separate power-down control is available for each speaker amp.

Parameter	Receiver Speaker Amp (EAR, XEAR)	Earphone Speaker Amp (JEAR)	Tone Amp (TONE)
Output type	BTL	Single	Single
Load resistance *1	32 Ω (typ.)	32 Ω (typ.)	600 Ω (typ.)
Load capacitance *2	0.1 µF	0.1 µF	
Maximum output power	10 mW (min.)	5 mW (min.)	

*1: Dynamic speaker

*2: A capacitor is required to prevent oscillation.

- **Analog output connection example**



Note: Insert C_1 capacitors of approximately 0.1 µF to prevent oscillation. C_2 is to cut DC.

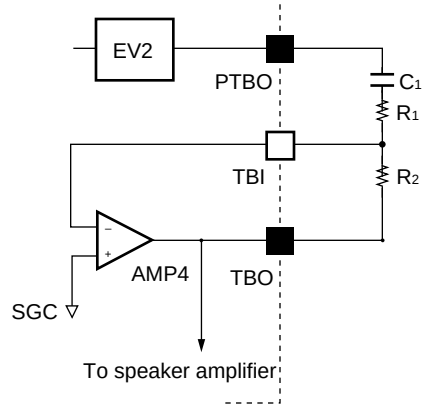
4. Reception Connections

This section describes reception connections, sidetone addition, and melody IC connection.

(1) Reception connections

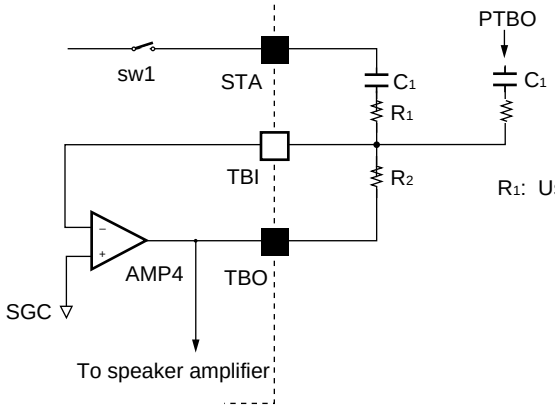
This describes the connection to the speaker amp for the reception signal.
Provide a high-pass filter at AMP4 to prevent a DC offset being applied to the speaker amp.

- **First-order high-pass filter**



(2) Sidetone addition

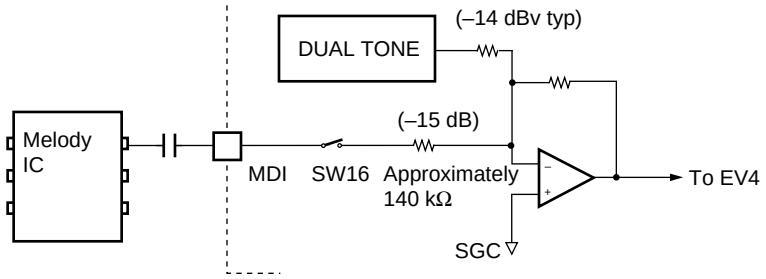
Sidetone addition is implemented by connecting the STA output and AMP4. In this case, use of a resistor of approximately 100 kΩ at AMP4 is recommended as the SW1 on resistance affects the sidetone gain.



R_1: Use a resistor of approximately 100 kΩ.

(3) Melody IC connection

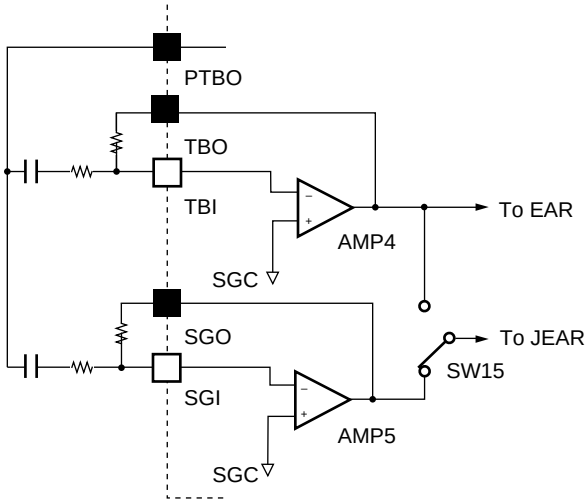
A melody IC can be connected using AMP4. However, the level can be made to vary in the same way as the tone if the MDI pin is used. MDI has an input impedance of approximately 140 kΩ and is not high impedance.



(4) JEAR signal selection

JEAR can receive a signal from AMP4 or AMP5. This enables a range of applications to be implemented depending on the AMP4 and AMP5 circuit structures.

- **Example of switching EAR and JEAR**



(5) Preventing a clicking sound when the electronic volume gain is changed or when muting

Changing the gain of the electronic volume or muting may result in a clicking sound due to fluctuation in the DC level. In such cases, the following setting is recommended.

Set the mode in which powering down the speaker amplifier is not linked with SW6b, 7b, 8b, and 9b (ADDRESS: 10001, DATA: 10111) and mute using SW6b, 7b, 8b, and 9b.

5. Power-Save Mode

This section describes the setting methods and states.

(1) Mode setting

Power-save mode can be controlled by an external control signal and register setting.

The various modes set each block to a power-save state, enabling the power consumption to be reduced.

- **Power-save mode setting table**

Mode	PS or Address 10111	Address														SYNC or CLK	VREF	AMP5	Transmission	CODEC	TONE	Reception				
		00100		00101	00110			10000				10001										EV2 AMP3, 4	Accessory	Ear Phone	TONE	Receiver
		D_4	D_0	D_4	D_2	D_1	D_0	D_4	D_3	D_2	D_1	D_4	D_2	D_1	D_0	STOP										
All PD	0	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	×	×	×	×	×	×	×	×	×	×
VREF operation	1	–	–	–	–	–	–	–	–	0	–	–	–	–	–	–	○	○	–	–	–	–	–	–	–	–
SGO PD	1	–	–	–	–	–	–	–	–	1	–	–	–	–	–	–	○	×	–	–	–	–	–	–	–	–
TONE operation	1	–	–	–	–	–	–	–	0	–	–	–	–	–	–	–	○	–	–	–	○	○	–	–	–	–
CODEC, TONE PD	1	–	–	–	–	–	–	1	1	–	–	–	–	–	–	–	○	–	–	×	×	×	×	×	×	×
CODEC operation	1	–	–	–	–	–	–	0	–	–	–	–	–	–	–	○	○	–	–	○	–	○	–	–	–	–
CODEC SYNC PD	1	–	–	–	–	–	–	0	–	–	–	–	–	–	–	×	○	–	–	×	–	○	–	–	–	–
Transmission operation	1	–	–	–	–	–	–	–	–	–	0	–	–	–	–	–	○	–	○	–	–	–	–	–	–	–
Transmission PD	1	–	–	–	–	–	–	–	–	–	1	–	–	–	–	–	○	–	×	–	–	–	–	–	–	–
Reception operation	1	1	–	1	1	1	1	0	1	–	–	0	1	0	0	–	○	–	–	○	–	○	×	○	×	×
	1	0	–	1	1	1	0	0	1	–	–	0	1	0	0	–	○	–	–	○	–	○	×	○	×	○
	1	0	–	1	1	0	1	0	1	–	–	0	0	0	1	–	○	–	–	○	–	○	×	×	○	○
	1	1	–	0	0	0	0	0	1	–	–	1	1	0	0	–	○	–	–	○	–	○	○	○	×	×
	1	0	–	1	1	1	1	0	1	–	–	1	1	1	1	–	○	–	–	○	–	○	○	○	○	○

○: Operation enabled, △: Changes depending on address 10001, ×: Power-down

Note: Powering down the CODEC or TONE generator powers down the entire reception block.

(2) Output pin states in each mode

Mode	PS or Address 10111	Address: 00100 D4	00100 D0	00101 D4	00101 D2	00101 D1	00101 D0	00110 D2	00110 D1	00110 D0	00111 D3	10000 D4	10000 D3	10000 D2	10000 D1	10000 D0	10001 D4	10001 D2	10001 D1	10001 D0	10010 D4	10010 D3	10010 D2	10010 D1	10010 D0	SYNC or CLK	Output Pin State: RAUD	EAR, XEAR	JEAR	TONE	TBO, PTBO	MICO, JMICO	BBO	STA	BTPO	SGC	SGO	DOUT	LO0 to 3
All PD	0																																					*
Reception mute	1	1	0	1				1	1	1	1					0	0	1	1	0		1				H	S	S	S	S	–	–	–	–	–	–	–	–	–
SGO PD	1	0		1				1	1	1				1		0	0	1	1	0						–	–	–	–	–	–	–	–	–	–	×	–	–	–
CODEC, TONE PD	1											1	1													–	×	×	×	×	R	–	–	R	○	–	H	–	–
Transmission PD	1													1												–	–	–	–	–	–	×	R 1	–	○	–	–	–	–
Transmission halt	–													0		1										–	–	–	–	–	–	–	–	–	–	–	H	–	–
Transmission mute	1		1		1	1	1							0							1	0				–	–	–	–	–	S	S	S	S	○	–	–	–	–
CODEC SYNC PD	1											0													STOP	–	–	–	–	–	–	–	–	–	–	H	–	–
CODEC operation	1											0													○	–	–	–	○	○	–	–	–	○	○	○	○	–	–
TONE operation	1												0													–	–	–	–	○	○	–	–	○	○	–	–	–	–
TONE mute	1																				1		1	1			–	–	S	–	–	–	–	–	○	–	–	–	–
TONE GND	1												1														–	–	G	–	–	–	–	–	–	–	–	–	–

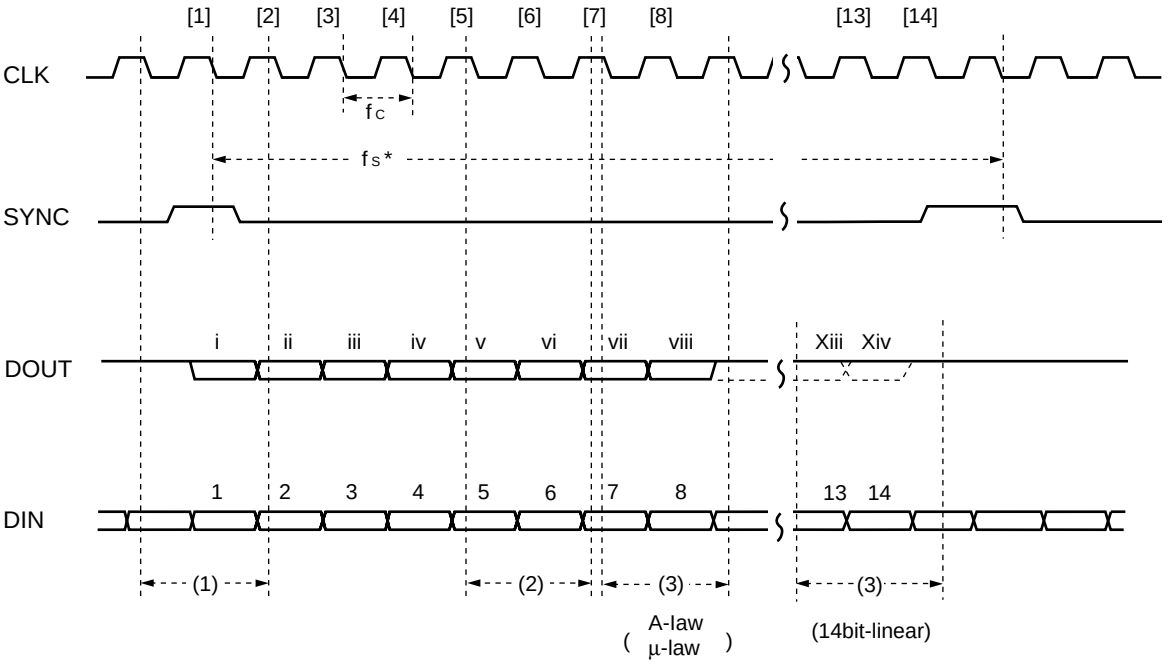
×: High impedance, S: Signal ground, R: Connected to signal ground via high resistance, ○: Normal operation

*: Depends on value of address 01000, G: Ground output, R1: Connected to signal ground via high resistance when SW1 is on.

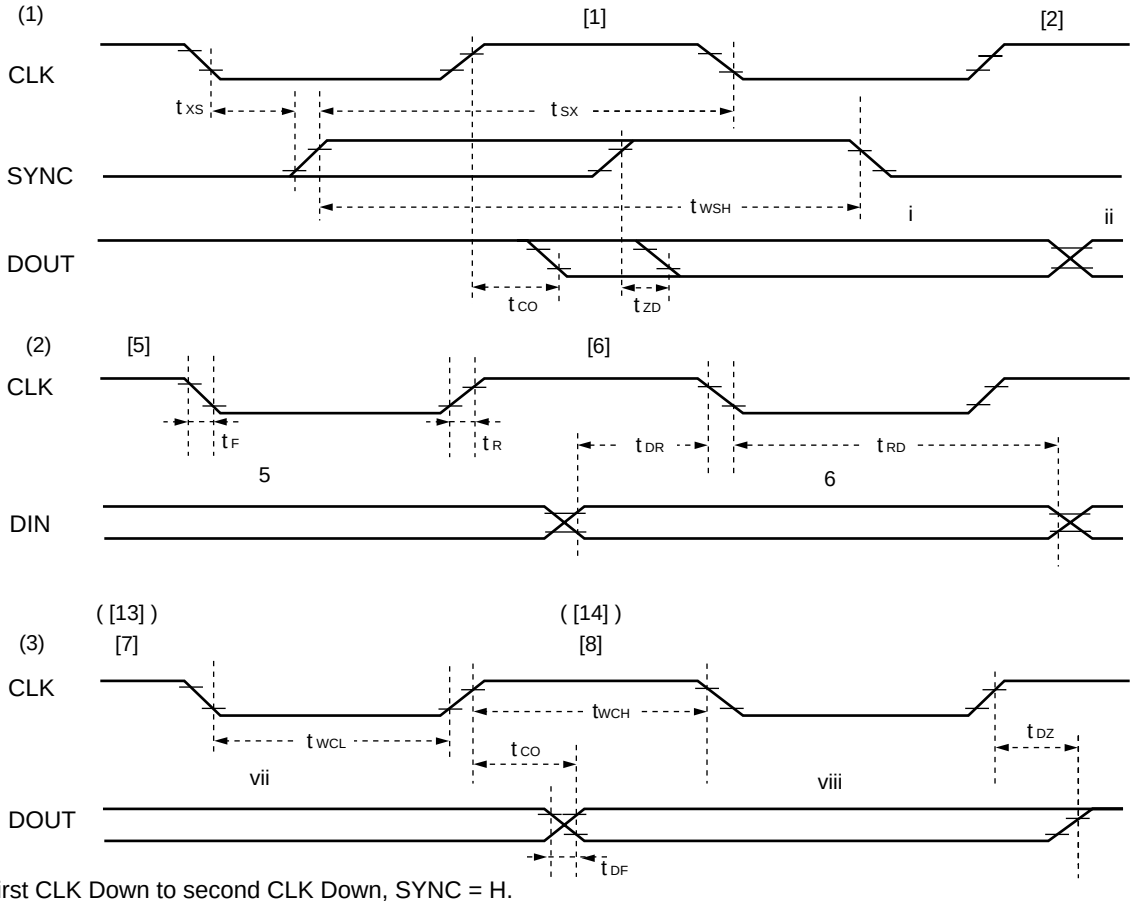
H: High level output

■ TIMING CHART

(1) Codec-Related Signals

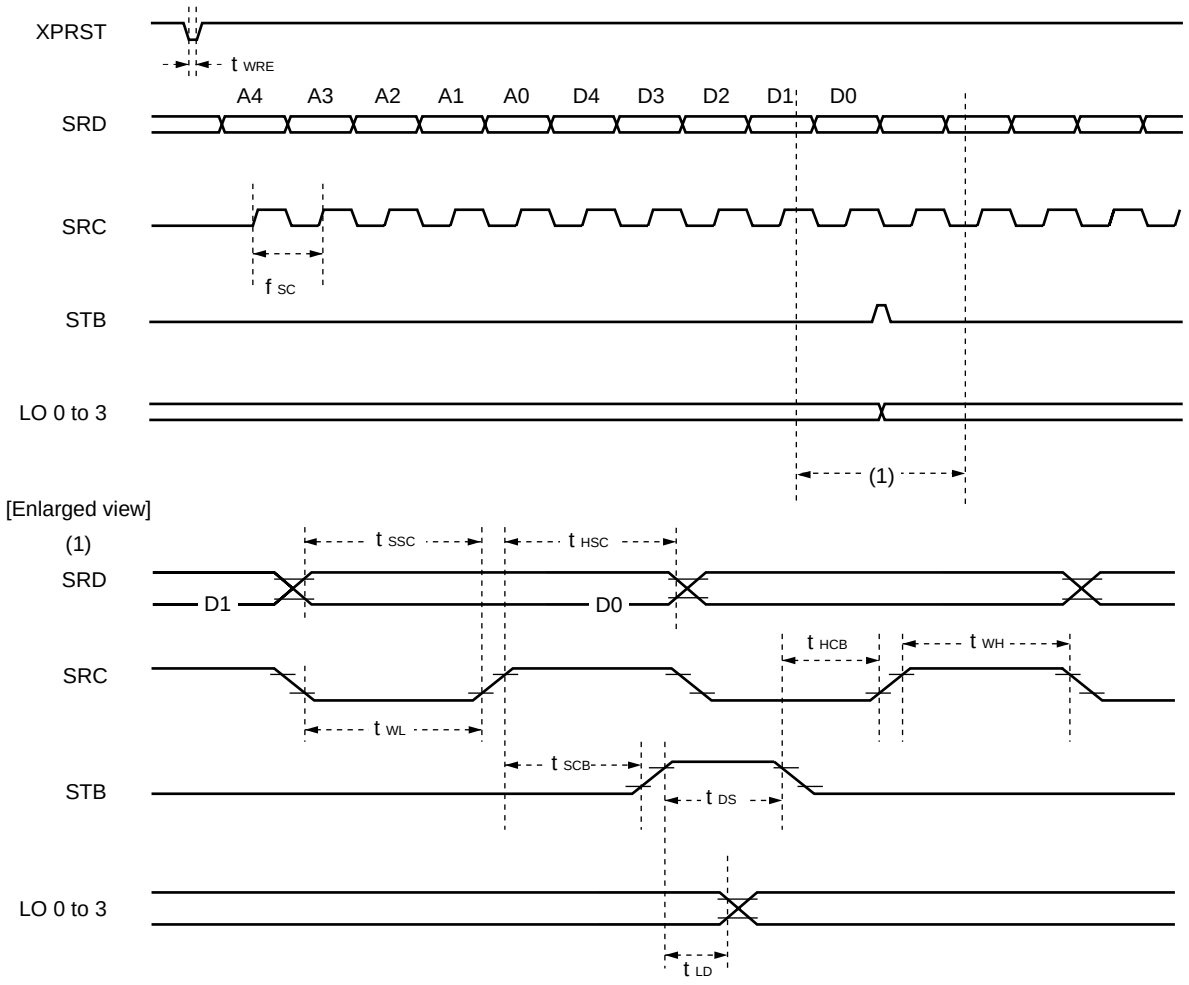


[Enlarged view]



*: From first CLK Down to second CLK Down, SYNC = H.

(2) Microcomputer Data-Related Signals



■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{DD}	–0.3	+6.0	V
Analog input voltage	V_{AIN}	–0.3	V_{DD} + 0.3	V
Digital input voltage	V_{DIN}	–0.3	V_{DD} + 0.3	V
Storage temperature	Tstg	–55	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Operating temperature	Ta	—	–20	25	80	°C
Power supply voltage	V_{DD}	VD1, VD2, VD3	2.7	3.0	3.6	V
"H" level digital input voltage	V_H	All digital input pins	$V_{DD} \times 0.7$	—	V_{DD}	V
"L" level digital input voltage	V_L		0.0	—	$V_{DD} \times 0.3$	V
Analog output load resistance	R_{LB}	*2	50	—	—	kΩ
Analog output load capacity	C_{LB}	BTPO, BBO, PTBO, TBO, SGO	—	—	20	pF
	C_{LS}	Between SGC-VS4	—	10	—	µF
Analog output load resistance*1	R_{LE}	Between EAR-XEAR	28	32	—	Ω
Analog output load capacity*1	C_{LE}	EAR, Between XEAR-GND	0.1	—	—	µF
Analog output load resistance*1	R_{LJ}	JEAR	28	32	—	Ω
Analog output load capacity*1	C_{LJ}	Between JEAR-GND	0.1	—	—	µF
Analog output load resistance	R_{LT}	TONE	600	—	—	Ω
Analog output load capacity	C_{LT}		—	—	100	pF
Analog output load resistance	R_{LM}	MICO, JMICO	10	—	—	kΩ
Analog output load capacity	C_{LM}		—	—	20	pF
Analog output load resistance	R_{LM}	RAUD	5	—	—	kΩ
Analog output load capacity	C_{LM}		—	—	20	pF
Analog output voltage	V_{AOUT}	All Amp. output pins	0.45	—	V_{DD}–0.45	V
Analog input voltage	V_{AIN}	All Amp. input pins	1.2	1.5	1.8	V
TCLK frequency	F_{TCLK}	TCLK	—	—	4.0	MHz

*1: Dynamic typ speakers

*2: BTPO, BBO, PTBO, TBO, SGC, SGO

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply current at full power-down mode	I_{PD}	All V_{DP} pins	PS = 0 Digital input = GND	—	0.5	50	µA
Power supply current for normal operation (all operation)	I_{VD2}		All blocks operating, CLK = 2048, SYNC = 8 kHz, no signal	—	5.0	10	mA
Digital input current	I_{IH}	All digital input pins	—	—	—	10	µA
	I_{IL}		—	—	—	10	µA
Digital output voltage	V_{OH}	All digital output pins	I_{OH} = –1.5 mA	V_{DD}×0.8	—	V_{DD}	V
	V_{OL}		I_{OL} = 1.5 mA	0.0	—	V_{DD}×0.2	V
Input offset voltage	V_{FM}	Between MIC-XMIC	MICO-MIC short	–10	—	10	mV
Output offset voltage	V_{FE}	Between EAR-XEAR	TBO-TBI short EV6 = 0 dB	–20	—	20	mV
SGC output voltage	V_{SGC}	SGC	—	1.40	1.50	1.60	V
Inter-pin resistance	R_{SW}	Between SWI-SWO	SW12 = on	—	—	2	kΩ
	R_{TE}	Between TAUD-EXSD	SW10 = on, SW11 = off, SW5 = off	—	—	2	kΩ
	R_{TD}	Between TAUD-DSCK	SW10 = off, SW11 = on, SW5 = off	—	—	2	kΩ
	R_{TG}	Between TONE-VS	SW14 = on	—	—	2	kΩ
	R_{BS}	Between BBO-STA	SW1 = on	—	—	2	kΩ
Input resistance	R_{ITA}	TAUD	Operating	70	100	140	kΩ
	R_{IMDA}	MDI	Operating, SW16 = ATT	100	140	200	kΩ
	R_{IMD}	MDI	Operating, SW16 = envelope	150	210	300	kΩ
Analog output off leak	I_{OFH}	RAUD, TONE	SW8a, SW9a, b, c, 14 = off, Vin = 0 to V_{DD}	–10	—	10	µA

Note: Measurement conditions: ■ Standard Test Circuit

2. AC Characteristics

(1) Codec-Related Signals

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Digital input rise time	t_R	$V_S \times 0.3 \rightarrow V_S \times 0.7$	—	—	50	ns
Digital input fall time	t_F		—	—	50	ns
Shift clock frequency	f_C	μ-law, A-law	64	—	3152	kHz
		Linear	128	—	3152	kHz
Shift clock pulse width (H)	t_{WCH}	$V_{IH} = V_S \times 0.7$	$1/f_C \times 0.3$	—	$1/f_C \times 0.7$	ns
Shift clock pulse width (L)	t_{WCL}	$V_{IL} = V_S \times 0.3$	$1/f_C \times 0.3$	—	$1/f_C \times 0.7$	ns
Sync frequency	f_S	—	—	8	—	kHz
Sync pulse width	t_{WSH}	—	$1/f_C$	—	62	μs
SYNC to CLK setup time	t_{SX}	—	100	—	—	ns
CLK to SYNC hold time	t_{XS}	—	50	—	—	ns
CLK to DIN hold time	t_{RD}	—	50	—	—	ns
DIN to CLK setup time	t_{DR}	—	50	—	—	ns
SYNC to DOUT delay time	t_{ZD}	BIT 1	—	—	200	ns
CLK to DOUT delay time	t_{CO}	BIT 2 to 8	—	—	200	ns
CLK to DOUT disable time	t_{DZ}	"H"	—	—	200	ns

(2) Microcomputer Data-Related Signals

Parameter	Symbol	Pin	Value			Unit
			Min.	Typ.	Max.	
SRC to SRD data setup time	t_{SSC}	SRD, SRC	50	—	—	ns
SRC to SRD data hold time	t_{HSC}		50	—	—	ns
SRC to STB setup time	t_{SCB}	SRC, STB	50	—	—	ns
SRC pulse width (H)	t_{WH}	SRC	200	—	—	ns
SRC pulse width (L)	t_{WL}		200	—	—	ns
STB pulse width	t_{DS}	STB	50	—	—	ns
STB to SRC hold time	t_{HCB}	STB, SRC	50	—	—	ns
LO0 to 3 delay time	t_{LD}	LO0 to 3	—	—	200	ns
Shift clock frequency	f_{SCLK}	SRC	—	—	2048	kHz
Reset pulse width	t_{WRE}	XPRST	1	—	—	μs

3. Transmission Characteristics

(1) Microphone Amp System

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain (between MICO and BBO)	G_{MB}	MICO = –20 dBV, 1020 Hz SW3 = on, SW1 = SW4 = SW5 = off EV0 = 0 dB	–1.5	—	1.5	dB
Gain (between JMICO and BBO)	G_{JB}	JMICO = –20 dBV, 1020 Hz SW4 = on, SW1 = SW3 = SW5 = off EV0 = 0 dB	–1.5	—	1.5	dB
Gain (between TAUD and BBO)	G_{TB}	TAUD = –20 dBV, 1020 Hz SW5 = on, SW1 = SW3 = SW4 = off EV0 = 0 dB	–1.5	—	1.5	dB
Signal to noise ratio (Microphone amp [1])	S_{MB}	Ain1 = –40 dBV (+20 dBgain), 1020 Hz SW3 = on, SW1 = SW4 = SW5 = off C message, Measured at MICO	40	—	—	dB
Signal to noise ratio (Microphone amp [2])	S_{JB}	Ain2 = –40 dBV (+20 dBgain), 1020 Hz SW4 = on, SW1 = SW3 = SW5 = off C message, Measured at JMICO	40	—	—	dB
Signal to noise ratio (BBO)	S_{TB}	TAUD = –40 dBV, 1020 Hz, SW5 = on, SW1 = SW3 = SW4 = SW10 = SW11 = off, EV0 = 0 dB, C message, Measured at BBO	40	—	—	dB

Note: Measurement conditions: ■ Standard Test Circuit

(2) Reception

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Gain Conditions: TBO = –20 dB, 1020 Hz	G_{TR}	Measured at RAUD	–1	0	1	dB
	G_{TE}	EV6 = 0 dB, Measured between EAR and XEAR	5	6	7	
	G_{TJ}	EV7 = 0 dB, Measured at JEAR	–1	0	1	
	G_{TT}	EV8 = 0 dB, SW9b = on, SW9c = off, Measured at TONE	–1	0	1	
Output power	P_E	R = 32 Ω, Between EAR and XEAR, EV6 = 0 dB, THD = 10%, 1020 Hz	10.0	—	—	mW
	P_J	R = 32 Ω, JEAR, EV7 = 0 dB, THD = 10%, 1020 Hz	5.0	—	—	mW
Signal to noise ratio	S_{TR}	TBO = –40 dBV, 1020 Hz, SW6b = SW7b = SW8b = SW9b = on, SW15 = AMP4, EV6, 7, 8 = 0 dB C message, RAUD, EAR-XEAR, Measured at JEAR	40	—	—	dB
	S_{TJ}	SGO = –40 dBV, 1020 Hz, SW7b = on, SW15 = AMP5, C message, Measured at JEAR	40	—	—	dB

Note: Measurement conditions: ■ Standard Test Circuit

(3) TONE

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
TONE output level	GT1	Generating 1 tone, f_1 = 948.1 kHz, sine wave SW2 = off, SW9b = off, SW9c = on, MDI = OPEN EV3 = 15 dB, EV4 = –15 dB, EV9 = 0 dB, Measured at TONE	–12.0	–14.0	–16.0	dBV
	GT2	Generating 2 tones, f_1 = 948.1 kHz, f_2 = 1219.1 kHz, simultaneous sine wave generation SW2 = off, SW9b = off, SW9c = on, MDI = OPEN EV3 = 15 dB, EV4 = –15 dB, EV9 = 0 dB, Measured at TONE	–12.0	–14.0	–16.0	dBV
	GT3	MDI = 1020 Hz, –10 dBV input SW2 = on, SW13 = off, DUAL TONE = off EV2 = 0 dB, EV3 = 15 dB, EV4 = –15 dB, EV5 = –14 dB, Measured at PTBO	–27.0	–29.0	–31.0	dB
Harmonic level	H_{TT}	EV3 = 15 dB, EV4 = –15 dB, EV9 = 0 dB, SW9c = on SW2 = SW9b = off, MDI = OPEN, Generating a single tone, Measured at TONE, nth harmonic level (n = 2 to 5)	—	—	–38	dB
	H_{TP}	EV3 = 15 dB, EV4 = –15 dB, EV5 = –15 dB, EV2 = 15 dB SW2 = on, SW9c = SW13 = off, MDI = OPEN, Generating a single tone, Measured at PTBO, nth harmonic level (n = 2 to 5)	—	—	–38	dB

(4) Reception and transmission (CODEC, Analog section)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Crosstalk (Transmission → reception)	CTX	Ain1 = 1020 Hz, –8.5 dBV (0 dBgain) D_{IN} = "H" Measurement: RAUD 1020 Hz	—	—	–50	dB
Crosstalk (Reception → transmission)	CTR	D_{IN} = 1020 Hz, 0 dBm 0 A_{IN} = SGC Measurement: DOUT 1020 Hz	—	—	–50	dB
Power supply noise rejection ratio	PSRR	0 < f < 50 kHz, V_{DD} + 30 mV_{OP} C message A_{IN} = SGC, D_{IN} = ICN	—	22	—	dB
Electronic volume gain error	GEV	EV0, EV1, EV3, EV5 Gain error relative to reset value Input = 1020 Hz, –20 dBV	–0.7	—	0.7	dB
		EV2, EV4, EV6, EV7, EV8, EV9 Gain error relative to reset value Input = 1020 Hz, –20 dBV	–1.0	—	1.0	dB

(Continued)

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Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Mute level	Gmsw2	SW2 = SW3 = off, EV4 = –15 dB EV2 = 0 dB, EV3 = 15 dB MDI = 1020 Hz, –30 dBV Measured at PTBO	—	—	–40	dB
	Gmsw34	SW1, 3, 4, 5 = off, EV0 = 0 dB AIN1 or AIN2 = 1020 Hz, –30 dBV Measured at BBO	—	—	–40	dB
	Gmsw5	SW1, 3, 4, 5 = off, EV0 = 0 dB TAUD = 1020 Hz, –30 dBV, Measured at BBO	—	—	–40	dB
	Gmsw69	SW6b = SW7b = SW8b = SW9b = SW9c = off EV6, 7, 8, 9 = 0 dB, TBO = 1020 Hz, –30 dBV MDI = 1020 Hz-30 dBV, EV4 = 0 dB RAUD, EAR, XEAR, JEAR, Measured at TONE	—	—	–40	dB
	Gmsw13	SW13 = SW2 = off, EV1, 2 = 0 dB, D_{IN} = 1020 Hz, 0 dBm0, Measured at PTBO	—	—	–40	dB
	Gmsw15a	SW15 = AMP4, TBI-TBO = short SGO = 1020 Hz, –30 dBV, Measured at JEAR	—	—	–40	dB
	Gmsw15b	SW15 = AMP5, SGI-SGO = short TBO = 1020 Hz, –30 dBV, Measured at JEAR	—	—	–40	dB
Electronic volume offset variation (amount of change for 1 step)	VEV0off (EV0)	SW3 = on, SW4 = SW5 = off MIC-MICO, SGC-XMIC = short Measured between SGC and BBO when EV0 variable	–10	—	10	mV
	VEV1off (EV1)	SW2 = off, SW13 = on, EV2 = 0 dB SYNC = 8 kHz, CLK = 2048 kHz, D_{IN} = ICN Measured between SGC and PTBO when EV1 variable	–25	—	25	mV
	VEV2off (EV2)	SW2 = off, SW13 = on, EV1 = 0 dB SYNC = 8 kHz, CLK = 2048 kHz, D_{IN} = ICN Measured between SGC and PTBO when EV2 variable	–25	—	25	mV
	VEV3off (EV3)	Tone generation = off, SW9a, 9b = off, SW9c = on, EV4 = –15 dB, EV9 = 0 dB, MDI = open Measured between SGC and TONE when EV3 variable	–70	—	70	mV
Electronic volume offset variation (amount of change for 1 step)	VEV4off (EV4)	Tone generation = off, MDI = open, EV3 = 15 dB, EV9 = 0 dB, SW9a = 9b = off, SW9c = on Measured between SGC and TONE when EV4 variable	–300	—	300	mV
	VEV5off (EV5)	Tone generation = off, MDI = open, EV3 = 15 dB, EV2 = 0 dB EV4 = –15 dB, SW2 = on, SW13 = off Measured between SGC and PTBO when EV5 variable	–5	—	5	mV

(Continued)

(Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Electronic volume offset variation (amount of change for 1 step)	VEV6off (EV6)	SW6b = on, SW6a = off TBI-TBO = short Measured between SGC and EAR when EV6 variable	–5	—	5	mV
	VEV7off (EV7)	SW7b = on, SW7a = off, SW15 = AMP4 TBI-TBO = short Measured between SGC and JEAR when EV7 variable	–5	—	5	mV
	VEV8off (EV8)	SW9b = on, SW9a, 9c = off TBI-TBO = short Measured between SGC and TONE when EV8 variable	–50	—	50	mV
	VEV9off (EV9)	Tone generation = off, MDI = open, EV3 = 15 dB EV4 = –15 dB, SW9c = on, SW9a, 9b = off Measured between SGC and TONE	–140	—	140	mV
Change in DC offset during mute	VSW2off (SW2)	SW13 = off, EV2 = 0 dB, EV3 = 15 dB, EV4 = –15 dB EV5 = –14 dB, Tone = off, MDI = open Measured at PTBO for SW2 on and off	–30	—	30	mV
	VSW3off (SW3)	SW1, 4, 5 = off, EV0 = 0 dB MIC-MICO = short Measured at BBO for SW3 on and off	–20	—	20	mV
	VSW4off (SW4)	SW1, 3, 5 = off, EV0 = 0 dB JMIC-JMICO = short Measured at BBO for SW4 on and off	–20	—	20	mV
	VSW5off (SW5)	SW1, 3, 4, 10, 11 = off, EV0 = 0 dB TAUD = SGC Measured at BBO for SW5 on and off	–10	—	10	mV
	VSW6off (SW6b)	SW7a, 8a, 9a = off, EV6 = –8 dB TBI-TBO = short, EV7 = –3 dB Measured at EAR, XEAR for SW6b on and off	–10	—	10	mV
	VSW7off (SW7b)	SW6a, 8a, 9a = off, SW15 = AMP4 EV7 = –3 dB, TBI-TBO = short Measured at JEAR for SW7b on and off	–10	—	10	mV
	VSW8off (SW8b)	SW6a, 7a, 9a = off TBI-TBO = short Measured at RAUD for SW8b on and off	–20	—	20	mV
	VSW9boff (SW9b)	SW6a, 7a, 8a, 9c = off, EV8 = 10 dB MDI = open, TBI-TBO = short Measured at TONE for SW9b on and off	–65	—	65	mV
	VSW9off (SW9c)	SW6a, 7a, 8a, 9b = off, EV9 = 6 dB MDI = open, TBI-TBO = short Measured at TONE for SW9c on and off	–300	—	300	mV
	VSWDoff (SW13)	SW2 = off, EV1, 2 = 0 dB, D_{IN} = ICN SYNC = 8 kHz, CLK = 2048 kHz Measured at PTBO for SW13 on and off	–90	—	90	mV

(5) Codec

Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Gain tracking (A to D) BTPO → DOUT	GTX	1020 Hz, –10 dBm0 Reference value (μ-law)	+3 to –40 dBm0	–0.3	—	0.3	dB
			–40 to –50 dBm0	–0.5	—	0.5	dB
			–50 to –55 dBm0	–1.0	—	1.0	dB
Gain tracking (D to A) DIN → PTBO	GTR	1020 Hz, –10 dBm0 Reference value (μ-law) EV1 = EV2 = 0 dB	+3 to –40 dBm0	–0.3	—	0.3	dB
			–40 to –50 dBm0	–0.5	—	0.5	dB
			–50 to –55 dBm0	–1.0	—	1.0	dB
Gain tracking (A to D) (Linear) BTPO → DOUT	GTXL	1020 Hz, AFST–13 dB Reference value	AFST to AFST–43 dB	–0.3	—	0.3	dB
			AFST–43 to AFST–53 dB	–0.5	—	0.5	dB
			AFST–53 to AFST–58 dB	–1.0	—	1.0	dB
Gain tracking (D to A) (Linear) DIN → PTBO	GTRL	1020 Hz, AFSR–13 dB Reference value EV1 = EV2 = 0 dB	AFSR to AFSR–43 dB	–0.3	—	0.3	dB
			AFSR–43 to AFSR–53 dB	–0.5	—	0.5	dB
			AFSR–53 to AFSR–58 dB	–1.0	—	1.0	dB
Transmitting frequency characteristics (A to D) BTPO → DOUT	FRX	0 dBm0 1020 Hz Reference value	0 to 60 Hz	24.0	—	—	dB
			60 to 300 Hz	–0.20	—	—	dB
			300 to 3000 Hz	–0.20	—	0.20	dB
			3000 to 3400 Hz	–0.20	—	0.8	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Receiving frequency characteristics (D to A) DIN → PTBO	FRR	0 dBm0 1020 Hz Reference value EV1 = EV2 = 0 dB	0 to 300 Hz	–0.30	—	—	dB
			300 to 3000 Hz	–0.30	—	0.30	dB
			3000 to 3400 Hz	–0.30	—	1.10	dB
			3400 to 4600 Hz	*	—	—	dB
			4600 to 12 kHz	32.0	—	—	dB
Transmitting absolute gain (A to D) BTPO → DOUT	GAX	1020 Hz, 0 dBm0 (Linear: AFST–3 dB) V_S = 3.0 V, Ta = +25°C		–1.0	0	1.0	dB
Receiving absolute gain (D to A) DIN → PTBO	GAR	1020 Hz, 0 dBm0 (Linear: AFSR–3 dB) EV1 = EV2 = 0 dB, V_S = 3.0 V, Ta = +25°C		–1.20	0	1.20	dB

*: $14.5 \times \{1 - \mathrm{Sin}\ \frac{\pi\ (4000 - f)}{1200}\ \}$

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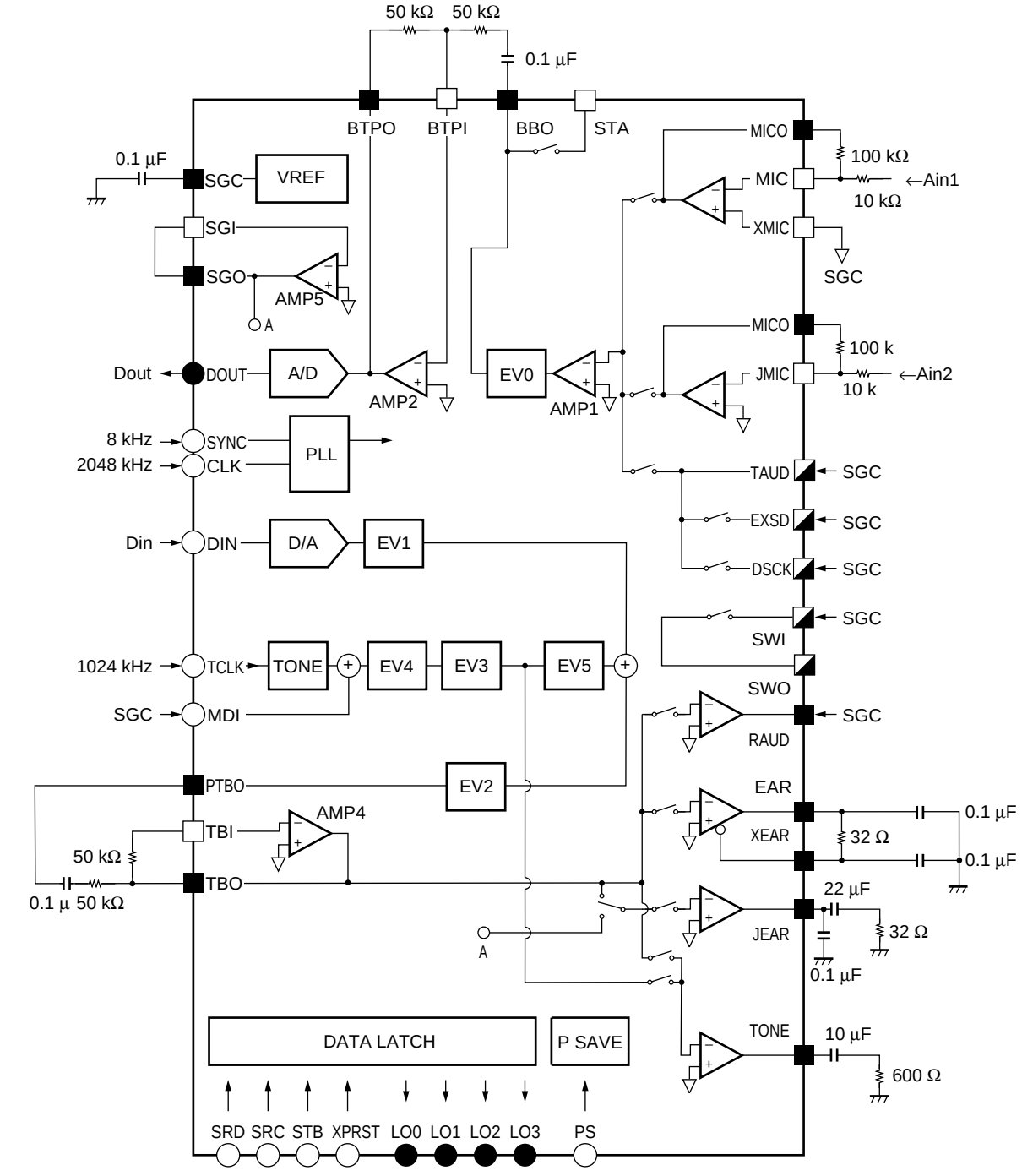
Parameter	Symbol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Transmitting signal to noise ratio (A to D) BTPO → DOUT	SDX	1020 Hz C message (μ-law)	0 to –30 dBm0	34.0	—	—	dB
			–40 dBm0	28.0	—	—	dB
			–45 dBm0	23.0	—	—	dB
Receiving signal to noise ratio (D to A) DIN → PTBO	SDR	1020 Hz C message EV1 = EV2 = 0 dB (μ-law)	0 to –30 dBm0	34.0	—	—	dB
			–40 dBm0	28.0	—	—	dB
			–45 dBm0	23.0	—	—	dB
Transmitting signal to noise ratio (A to D) BTPO → DOUT (Linear)	SDXL	1020 Hz C message	AFST–3 to AFST–33 dB	34.0	—	—	dB
			AFST–43 dB	28.0	—	—	dB
			AFST–48 dB	23.0	—	—	dB
Recieving signal to noise ratio (D to A) SDRL DIN → PTBO (Linear)	SDRL	1020 Hz C message EV1 = EV2 = 0 dB	AFSR–3 to AFSR–33 dB	34.0	—	—	dB
			AFSR–43 dB	28.0	—	—	dB
			AFSR–48 dB	23.0	—	—	dB
Transmitting no-talk noise BTPO → DOUT	ICNX	C message		—	–72	–69	dBm0C
Receiving no-talk noise DIN → PTBO	ICNR	C message EV1 = EV2 = 0 dB		—	–75	–70	dBm0C
Analog input level BTPO	AILU	1020 Hz, 0 dBm0, Ta = +25°C V_S = 3.0 V μ-law		0.3290	0.3739	0.4195	Vrms
Analog output level PTBO	AOLU	1020 Hz, 0 dBm0, Ta = +25°C V_S = 3.0 V μ-law EV1 = EV2 = 0 dB		0.3290	0.3739	0.4195	Vrms
Analog input fullscale level BTPO	AFST	V_S = 3.0 V, Ta = +25°C Linear		0.6729	0.7647	0.8581	V_{OP}
Analog output fullscale level PTBO	AFSR	V_S = 3.0 V, Ta = +25°C Linear EV1 = EV2 = 0 dB		0.6729	0.7647	0.8581	V_{OP}

■ TEST CIRCUIT



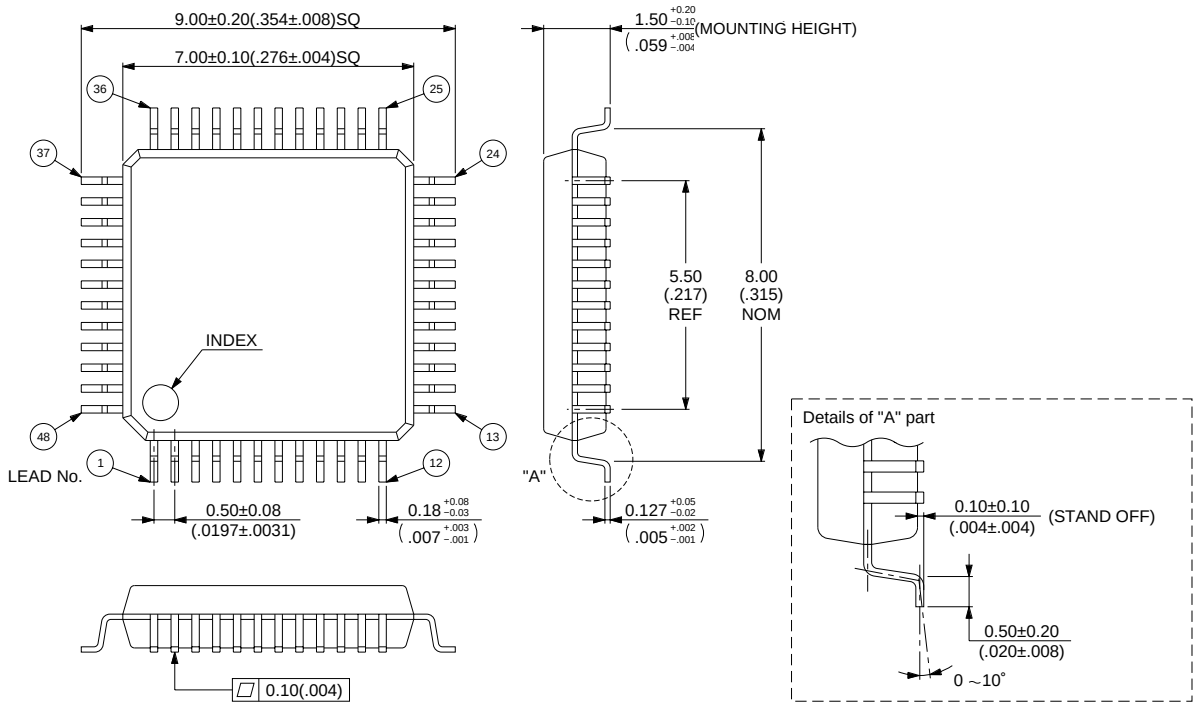
Note: Insert a large bypass capacitor between VD and GND and between SGC and VS4.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB86437PFV	48 pins, Plastic LQFP (FPT-48P-M05)	

■ PACKAGE DIMENSION

48 pin Plastic LQFP
(FPT-48P-M05)



Dimensions in mm (inches)

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